PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Ichio YUDASAKA, Tatsuya SHIMODA, Sadao KANBE and Wakao MIYAZAWA

Application No.: 09/901,126

Filed: July 10, 2001 Docket No.: 040090.02

For: THIN FILM DEVICE PROVIDED WITH COATING FILM, LIQUID CRYSTAL PANEL AND ELECTRONIC DEVICE, AND METHOD FOR MAKING THE THIN FILM DEVICE

REQUEST FOR DECLARATION OF INTERFERENCE

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Applicants hereby respectfully request that an Interference be declared between the above-identified patent application and United States Patent No. 6,087,196 to Sturm et al. (hereinafter "Sturm"), attached to the Information Disclosure Statement filed on July 10, 2001.

Specifically, the Applicants request that an Interference be declared between claims 82, 83, and 111-113 of the present Application and claims 23-29 of Sturm.

Additionally, the Applicants propose that count 3 set forth in Appendices A and B, be made the count of the Interference. The count is numbered 3 to avoid confusion with other counts (numbered differently) of Interferences in Applicants' other Applications, in which corresponding Requests for Declaration of Interference and a Petition for Consolidation of Three Interferences are being concurrently filed.[1]

[1] United States Patent Applications with Serial Numbers 09/901,097 and 09/901,095 are the other Applications in which concurrent Requests for Declaration of Interference are being filed.

Moreover, the Applicants respectfully request that claims 82, 83, and 111-113 of the present Application and claims 23-29 of Sturm be designated as corresponding to count 3.

The Applicants note that claim 111 of the present Application corresponds exactly to count 3. Claim 23 of Sturm and claim 82 of the present Application are identical and both would have been obvious over count 3 (and count 3 is anticipated by them). Additionally, claim 23 of Sturm broadly recites the semiconducting polymer layer and has a scope encompassed by claim 112 of the present Application.

Claim 24 of Sturm and claim 83 of the present Application are identical and may suffer from 35 U.S.C. §112, second and fourth paragraph, problems, correcting which problems may yield claim 113 of the present Application.

Claims 25-29 of Sturm recite further features that would have been obvious over claim 23 of Sturm, which would make them obvious over count 3 and over claim 82 of this Application.

Attached Appendix A shows the support for features of claims 82, 83, and 111-113 in the present Application. Attached Appendix A also shows the support in Japanese Priority Document, JP 8-120653, filed in Japan on May 15, 1996, for proposed features recited in interference count 3. Attached Appendix B lays out the rationale for correspondence between count 3, claims 82, 83, and 111-113 of the present Application, and claims 23-29 of Sturm.

Furthermore, the Applicants respectfully request that the Examiner acknowledge in the Declaration of Interference Applicants' right to the benefit of PCT/JP 97/01618, filed May 14, 1997. Additionally, the Applicants respectfully request that the Examiner acknowledge in the Declaration of Interference Applicants' right to the benefit of their Japanese Priority Document, JP 8-120653, filed in Japan on May 15, 1996.

Applicants respectfully submit that all of the claims pending in this Application meet the requirements of 35 U.S.C. §135(b), and therefore satisfy 37 C.F.R. §1.607(a)(6), because

the preliminary amendment filed on July 10, 2001 (less than one year after issue date of Sturm) presented claims to the same subject matter as claims added after July 11, 2001.

In accordance with 37 C.F.R. §1.607(b), the Applicants respectfully request that examination of the present Application be conducted with special dispatch within the Patent and Trademark Office. Attention is respectfully directed to the Petition for Consolidation of Three Interferences, a copy of which is attached.

Should there be any questions concerning this communication, please telephone the undersigned at the number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Hrayr A. Sayadian
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JAO:HAS/tbh

Attachments:
Appendix A
Appendix B
Petition

Date: February 27, 2002

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Count	Claim in '196 Patent	Claims in 09/901,126	Support in 09/901,126	Support in Priority Doc JP 8-120653
Count 3. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	23. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a polymer semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	82. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a polymer semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	Fig. 38(B), P93, L1-4: reverse stagger-type TFT. Fig. 38(B), P93, L1-P94, L21: - insulating substrate 410 and protective underlayer 411. - gate electrode 415. - gate insulating film 413. - amorphous silicon film 417. - source/drain electrodes 431, 492. P94, L22, P95, L4: Semiconducting layer can be formed of a coating film as in the first embodiment. P41-42: using polymer silane having various plural monomer units as the material forming the conductive layer; P58, L5-9: using ink-jetting to deposit the material forming the conductive layer. Figs. 14-16; P56, L1-P59, L21: Ink-jet printing also, applicable to the silicon film forming the channel region (region 14C between 14S and 14D in Fig. 10). See P58, L5-9.	P24, ¶42 through page 26 ¶44 describes the TFT and its components (by reference to Figures 3 and 4, including an insulating substrate 401, a gate electrode 405, gate insulating film 404, semiconducting channel region 403, source contacts 403S, and drain contacts 403D), wherein the channel region is formed from polymer silane having various plural monomer units as the material forming the polymer semiconducting layer; P39, ¶39 describes using ink-jetting to form the channel and the insulating film.

Count	Claim in '196 Patent	Claims in 09/901,126	Support in 09/901,126	Support in Priority Doc JP 8-120653
3	24. The process of claim 23 wherein said gate insulator is formed by ink-jet printing, and the semiconducting layer by other techniques.	83. The process of claim 82 wherein said gate insulator is formed by ink-jet printing, and the semiconducting layer by other techniques.	P94, L22-P95, L4; Figs. 14-16; and P56, L1-P59, L2.	
Count 3. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.		111. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	Fig. 38(B), P93, L1-4: reverse stagger-type TFT. Fig. 38(B), P93, L1-P94, L21: - insulating substrate 410 and protective underlayer 411. - gate electrode 415. - gate insulating film 413. - amorphous silicon film 417. - source/drain electrodes 431, 492. P94, L22, P95, L4: semiconducting layer can be formed of a coating film as in the first embodiment. Figs. 14-16; P56, L1-P59, L21: Ink-jet printing also, applicable to the silicon film forming the channel region (region 14C between 14S and 14D in Fig. 10). See P58, L5-9.	P24, ¶42 through page 26 ¶44 describes the TFT and its components (by reference to Figures 3 and 4, including an insulating substrate 401, a gate electrode 405, gate insulating film 404, semiconducting channel region 403, source contacts 403S, and drain contacts 403D), wherein the channel region is a semiconductor formed from polymer silane having various plural monomer units as the material forming the semiconducting layer; P39, ¶39 describes using ink-jetting to form the channel and the insulating film.

Count	Claim in '196 Patent	Claims in 09/901,126	Support in 09/901,126	Support in Priority Doc JP 8-120653
3		112. The process of claim 111 wherein said formed semiconducting layer has a molecular structure containing plural monomer units.	P41-42: using silane having various plural monomer units as the material forming the conductive layer; P58, L5-9: using ink-jetting to deposit the material forming the conductive layer.	
3		113. The process of claim 82 wherein said gate insulator is formed by ink-jet printing.	P94, L22-P95, L4; Figs. 14-16; and P56, L1-P59, L2.	

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
23. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a polymer semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	82. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a polymer semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	3	Claim 82 of this Application is a copy of claim 23 of the '196 patent Claim 82 of this Application does not explicitly disclose forming a polymer semiconducting layer on said insulator by ink-jet printing. However, it would have been obvious to use a polymer semiconducting layer as the semiconducting layer to achieve stable and low voltage transistor operation. See, e.g., the abstract in Aratani '139 disclosing using organic thin film semiconducting layers instead of silicon semiconductors to achieve a stable, long life, and low voltage devices. Additionally, features of claim 82 of this Application are anticipated by features of claim 23 of the '196 patent.	Count 3 does not recite forming a polymer semiconducting layer on said insulator by ink-jet printing. However, it would have been obvious to replace the semiconducting layer by a polymer semiconducting layer to achieve stable and low voltage transistor operation in an inexpensive manner. See, e.g., Ebisawa (1983), and Japanese Unexamined Publication Nos. (JP-A) 62-311174 and 62-85224. See, also the abstract in Aratani '139 disclosing using organic thin films instead of semiconductors to achieve a stable, long life, and low voltage devices. Additionally, features of count 3 are anticipated by features of claim 23 of the '196 patent and claim 82 of this Application.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
24. The process of claim 23 wherein said gate insulator is formed by ink-jet printing, and the semiconducting layer by other techniques.	83. The process of claim 82 wherein said gate insulator is formed by ink-jet printing, and the semiconducting layer by other techniques.	3	Claim 83 of this Application is a copy of claim 24 of the '196 patent	Count 3 does not recite forming the gate insulator by ink-jet printing. However, it would have been obvious to form the gate insulator using ink-jet printing. See, e.g., Drummon '248 disclosing ink-jet depositing various materials including insulators because the depositing by the ink-jet method is less expensive and simple, see, e.g., column 4, lines 40-55. Additionally, it would have been obvious to use ink-jet printing because the semiconducting layer is formed above the gate insulator and it would simplify the processing to use ink-jet printing to form both elements. Moreover, it would have been obvious to replace the semiconducting layer by a polymer semiconducting layer to achieve stable and low voltage transistor operation in an inexpensive manner. See, e.g., Ebisawa (1983), and Japanese Unexamined Publication Nos. (JP-A) 62-311174 and 62-85224. See, also the abstract in Aratani '139 disclosing using organic thin films instead of semiconductors to achieve a stable, long life, and low voltage devices. Additionally, features of count 3 are anticipated by features of claim 24 of the '196 patent and claim 83 of this Application.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
23. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a polymer semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	111. A process of forming thin film field effect transistors comprising the steps of: forming a gate electrode on a substrate; forming a gate insulator over said gate electrode; forming a semiconducting layer on said insulator by ink-jet printing; and forming source and drain contacts on said semiconducting layer.	3	Claim 111 of this Application does not explicitly disclose forming a polymer semiconducting layer on said insulator by ink-jet printing. However, it would have been obvious to replace the semiconducting layer by a polymer semiconducting layer to achieve stable and low voltage transistor operation in an inexpensive manner. See, e.g., Ebisawa (1983), and Japanese Unexamined Publication Nos. (JP-A) 62-311174 and 62-85224. See, also the abstract in Aratani '139 disclosing using organic thin films instead of semiconductors to achieve a stable, long life, and low voltage devices. Additionally, features of claim 111 of this Application are anticipated by features of claim 23 of the '196 patent.	Claim 111 of this Application is a copy of Count 3.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
	112. The process of claim 111 wherein said formed semiconducting layer has a molecular structure containing plural monomer units.	3	The broad recitation of polymer in claim 23 of the '196 patent makes claim 112 of this Application anticipate claim 23 of the '196 patent, and vise-versa.	Count 3 does not recite forming a semiconducting layer on said insulator by ink-jet printing, wherein said formed semiconducting layer has a molecular structure containing a polymer consisting of plural monomer units. However, it would have been obvious to replace the semiconducting layer by a semiconducting layer has a molecular structure containing a polymer consisting of plural monomer units to achieve stable and low voltage transistor operation in an inexpensive manner. See, e.g., Ebisawa (1983), and Japanese Unexamined Publication Nos. (JP-A) 62-311174 and 62-85224. See, also the abstract in Aratani '139 disclosing using organic thin films instead of semiconductors to achieve a stable, long life, and low voltage devices. Additionally, features of count 3 are anticipated by features of claim 23 of the '196 patent and claim 112 of this Application.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
	113. The process of claim 82 wherein said gate insulator is formed by ink-jet printing.	3	Claim 24 of the '196 patent may suffer 35 U.S.C. §112, second and fourth paragraphs, problems, correcting which problem may lead to a claim similar to claim 113 of the present Application.	Count 3 does not recite forming the gate insulator by ink-jet printing. However, it would have been obvious to form the gate insulator using ink-jet printing. See, e.g., Drummon '248 disclosing ink-jet depositing various materials including insulators because the depositing by the ink-jet method is less expensive and simple, see, e.g., column 4, lines 40-55. Additionally, it would have been obvious to use ink-jet printing because the semiconducting layer is formed above the gate insulator and it would simplify the processing to use ink-jet printing to form both elements. Moreover, it would have been obvious to replace the semiconducting layer by a polymer semiconducting layer to achieve stable and low voltage transistor operation in an inexpensive manner. See, e.g., Ebisawa (1983), and Japanese Unexamined Publication Nos. (JP-A) 62-311174 and 62-85224. See, also the abstract in Aratani '139 disclosing using organic thin films instead of semiconductors to achieve a stable, long life, and low voltage devices. Additionally, features of count 3 are anticipated by features of claim 113 of this Application.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
25. The process of claim 23 wherein the source and drain contacts are applied directly on the gate insulator before the semiconducting layer is deposited.		3	The analysis above with respect to claim 23 of the '196 patent is incorporated herein. Additionally, it is notoriously well known practice in the semiconductor processing art to perform as much of the same processing together as possible to economize on wasteful process change preparations. Consequently, it would have been obvious to apply the source and drain before depositing the semiconducting layer. Additionally, features of claim 82 of this Application are anticipated by features of claim 25 of the '196 patent.	It is notoriously well known practice in the semiconductor processing art to perform as much of the same processing together as possible to economize on wasteful process change preparations. Consequently, it would have been obvious to apply the source and drain before depositing the semiconducting layer. Additionally, features of count 3 are anticipated by features of claim 25 of the '196 patent.
26. The process of claim 24 wherein the source and drain contacts are applied directly on the gate insulator before the semiconducting layer is deposited.		3	The analysis above with respect to claim 24 of the '196 patent is incorporated herein. Additionally, it is notoriously well known practice in the semiconductor processing art to perform as much of the same processing together as possible to economize on wasteful process change preparations. Consequently, it would have been obvious to apply the source and drain before depositing the semiconducting layer. Additionally, features of claim 83 of this Application are anticipated by features of claim 26 of the '196 patent.	It is notoriously well known practice in the semiconductor processing art to perform as much of the same processing together as possible to economize on wasteful process change preparations. Consequently, it would have been obvious to apply the source and drain before depositing the semiconducting layer. Additionally, features of count 3 are anticipated by features of claim 26 of the '196 patent.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
27. The process of claim 23 wherein the semiconducting layer comprises a non-polymeric organic film or a polymer/small organic molecule blend.		3	The analysis above with respect to claim 23 of the '196 patent is incorporated herein. Additionally, claim 82 of this Application does not explicitly disclose mixing a polymer with other organic molecules. However, it is well known to use a blend of polymer with other organic molecules including dyes with small molecular structure, instead of separate layers, to use a single deposition step and thus simplify the deposition process and produce electro-luminescent element exhibiting excellent luminescence efficiency and brightness even at low voltage and low current density. See, e.g., Mori '489, col. 2, line 66, to col. 3, line 46 and Example 1 in column 30 lines 54-63, disclosing the use of blend of a polymer and a small organic molecule; see also, e.g., Vestweber (1994), the second paragraph in section titled Introduction on p. 141, stating that polymer blends consisting of a mixture of a charge transport component and a polymeric binder offers the advantage of combining easy spectral tuning by appropriate selection of the active component with the processibility and good mechanical properties of molecules.. Additionally, features of claim 82 of this Application are anticipated by features of claim 27 of the '196 patent.	Count 3 does not recite mixing a polymer with other organic molecules. However, it is well known to use a blend of polymer with other organic molecules including dyes with small molecular structure, instead of separate layers, to use a single deposition step and thus simplify the deposition process. See, e.g., Mori '489, column 3 lines 22-46 and Example 1 in column 30 lines 54-63, disclosing the use of blend of a polymer and a small organic molecule; see also, e.g., Vestweber (1994), the second paragraph in section titled Introduction on p. 141. Additionally, features of count 3 are anticipated by features claim 27 of the '196 patent.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
28. The process of claim 24 wherein the semiconducting layer comprises a non-polymeric organic film or a polymer/small organic molecule blend.		3	The analysis above with respect to claim 24 of the '196 patent is incorporated herein. Additionally, claim 83 of this Application does not explicitly disclose mixing a polymer with other organic molecules. However, it is well known to use a blend of polymer with other organic molecules including dyes with small molecular structure, instead of separate layers, to use a single deposition step and thus simplify the deposition process. See, e.g., Mori '489, column 3 lines 22-46 and Example 1 in column 30 lines 54-63, disclosing the use of blend of a polymer and a small organic molecule; see also, e.g., Vestweber (1994), the second paragraph in section titled Introduction on p. 141. Additionally, features of claim 83 of this Application are anticipated by features of claim 28 of the '196 patent.	Count 3 does not recite mixing a polymer with other organic molecules. However, it is well known to use a blend of polymer with other organic molecules including dyes with small molecular structure, instead of separate layers, to use a single deposition step and thus simplify the deposition process. See, e.g., Mori '489, column 3 lines 22-46 and Example 1 in column 30 lines 54-63, disclosing the use of blend of a polymer and a small organic molecule; see also, e.g., Vestweber (1994), the second paragraph in section titled Introduction on p. 141. Additionally, features of count 3 are anticipated by features of claim 28 of the '196 patent.

Claims in '196 Patent	Claims in 09/901,126	Correspond to count No.	Rationale for Correspondence Between Claims of '196 Patent and the Claims in 09/901,126	Rationale for Correspondence Between the Claims and the Count
29. The process of claim 25 wherein the semiconducting layer comprises a non-polymeric organic film or a polymer/small organic molecule blend.		3	The analysis above with respect to claim 25 of the '196 patent is incorporated herein. Additionally, claim 82 of this Application does not explicitly disclose mixing a polymer with other organic molecules. However, it is well known to use a blend of polymer with other organic molecules including dyes with small molecular structure, instead of separate layers, to use a single deposition step and thus simplify the deposition process. See, e.g., Mori '489, column 3 lines 22-46 and Example 1 in column 30 lines 54-63, disclosing the use of blend of a polymer and a small organic molecule; see also, e.g., Vestweber (1994), the second paragraph in section titled Introduction on p. 141. Additionally, features of claim 82 of this Application are anticipated by features of claim 29 of the '196 patent.	Count 3 does not recite mixing a polymer with other organic molecules. However, it is well known to use a blend of polymer with other organic molecules including dyes with small molecular structure, instead of separate layers, to use a single deposition step and thus simplify the deposition process. See, e.g., Mori '489, column 3 lines 22-46 and Example 1 in column 30 lines 54-63, disclosing the use of blend of a polymer and a small organic molecule; see also, e.g., Vestweber (1994), the second paragraph in section titled Introduction on p. 141. Additionally, features of count 3 are anticipated by features of claim 29 of the '196 patent.

COPY

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Satoru MIYASHITA, Hiroshi KIGUCHI, Tatsuya SHIMODA and Sadao KANBE

Application No.: 09/901,097

Filed: July 10, 2001 Docket No.: 101050.02

For: METHOD OF MANUFACTURING ORGANIC EL ELEMENT, ORGANIC EL ELEMENT, AND ORGANIC EL DISPLAY DEVICE

PETITION FOR CONSOLIDATION OF THREE INTERFERENCES

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

This is a petition under 37 C.F.R. §1.182 requesting that three requested interference proceedings be consolidated. Specifically, this Petition requests the consolidation of the interferences resulting from three Requests for Declaration of Interference, concurrently filed in the above-identified Application and co-pending United States Patent Applications having Serial Numbers 09/901,095 and 09/901,126, seeking the declaration of interference between the above mentioned three applications and United States Patent No. 6,087,196 to Sturm et al. (hereinafter "Sturm").

The Applicants respectfully submit that considerations of efficiency, uniformity, expense, and speed in prosecuting the interferences between the above-identified Applications and Sturm can best be satisfied by consolidating the three Requests for Declaration of Interference and collectively and concurrently prosecuting a single interference between Sturm and the above-identified Applications. See the preamble of 37 C.F.R. §1.601 defining a primary

good of the rules as being to secure the just, speedy, and inexpensive determination of every interference.

In each of the above-referenced Applications, a Request for Declaration of Interference with Sturm is filed.

Additionally, the above-referenced Applications and Sturm are directed to similar subject matter. Broadly speaking, the three Applications and Sturm disclose using ink-jet printing to form semiconducting devices including organic semiconducting elements or including polymeric elements. Indeed, Applications with Serial Numbers 09/901,097 and 09/901,095 include claims exactly, and claims substantially, corresponding to each of interference counts 1 and 2 with corresponding claims of Sturm.

Moreover, the above-identified Applications are assigned to a common assignee.

Accordingly, disputed issues between the three Applications and Sturm address similar subject matter between the same two parties.

Therefore, to efficiently, uniformly, and speedily prosecute the Interference between the above-identified Applications and Sturm, the Applicants respectfully request:

(1) That the three Requests for Declaration of Interference be consolidated, and

(2) That the resulting interference proceedings between Sturm and the above-referenced three Applications be consolidated.

Application No. 09/901,097

Attached is our check no. 128238, in the amount of $130.00, as the petition fee set forth in 37 C.F.R. §1.17(h). If any additional fees are necessary, the U.S. Patent and Trademark Office is authorized to debit Deposit Account No. 15-0461.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Hrayr A. Sayadian
Registration No. 46,491

JAO:HAS/tbh

Date: February 27, 2002

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